AMENDMENTS TO THE CLAIMS

1. (Withdrawn) A method for forming an interconnecting substrate, comprising

providing a support base,

disposing on said support base a decoupling capacitor, and

employing a deposition process to form an interconnect layer over said decoupling capacitor, whereby an interconnecting substrate is formed having an embedded decoupling capacitor.

2. (Withdrawn) A method according to claim 1, including forming electrical connections on a surface of said interconnect layer and extending into said interconnect layer, thereby allowing devices to be mounted on said surface of said interconnect layer.

3. (Withdrawn) A method according to claim 1, wherein employing a deposition process to form an interconnect layer includes forming an interconnect layer having a power and a ground plane.

4. (Withdrawn) A method according to claim 1, wherein employing a deposition process to form an interconnect layer includes forming an interconnect layer having a plurality of signal planes.

5. (Withdrawn) A method according to claim 1, wherein disposing on said support base a decoupling capacitor includes disposing on said support base a plurality of decoupling capacitors.

6. (Withdrawn) A method according to claim 1, wherein disposing on said support base a decoupling capacitor includes disposing on said support base a plurality of decoupling capacitors having a common ground plane.

7. (Withdrawn) A method according to claim 1, wherein disposing on said support base a decoupling capacitor includes forming a capacitor on said support base.

8. (Withdrawn) A method according to claim 1, including disposing on said support base a terminating resistor.

9. (Withdrawn) A method according to claim 1, including disposing a device on a surface of said interconnect layer at locations selected to reduce an interconnect length between said device and said decoupling capacitor.

10. (Withdrawn) A method according to claim 1, including wire bonding devices to a surface of said interconnect layer.

11. (Withdrawn) A method according to claim 1, including flip-chip mounting devices to a surface of said interconnect layer.

12. (Currently amended) A device for interconnecting a plurality of circuit devices, comprising:

a decoupling capacitor mounted on a first surface and having a grounding pad and a power pad formed on a top surface of said decoupling capacitor; and

an interconnect layer having a pattern of circuit connections and being formed over said top surface of said decoupling capacitor, whereby electrical connections to ~~of~~ said decoupling capacitor are embedded within said interconnect layer and said interconnect layer is disposed between said decoupling capacitor and said plurality of circuit devices,

and whereby said pattern of circuit connections of said interconnect layer is coupled to said decoupling capacitor and said plurality of circuit devices, said pattern of circuit connections coupling to said grounding pad and said power pad of said decoupling capacitor.

13.-20. Cancelled.

21. (Previously presented) The device according to claim 12, wherein said pattern of circuit connections includes at least one of the following to interconnect said plurality of circuit devices: a signal plane, a power plane and a ground plane.

22. (Previously presented) The device according to claim 12, wherein said interconnect layer includes a power plane and a ground plane, and wherein said decoupling capacitor connects in parallel between said power and ground planes.

23. (Cancelled)

24. (Previously presented) The device according to claim 12, wherein said decoupling capacitor comprises a silicon containing dielectric material.

25. (Previously presented) The device according to claim 12, wherein said interconnecting layer comprises a plurality of aluminum containing conductive paths.

26. (Previously presented) The device according to claim 12, wherein said interconnecting layer comprises a plurality of copper containing conductive paths.

27. (Previously presented) The device according to claim 12, wherein said decoupling capacitor comprises a silicon base die decoupling capacitor.

28. (Previously presented) The device according to claim 12, said decoupling capacitor having a capacitance in the range of 1 to 1000 nf/cm^2.

29. (Previously presented) The device according to claim 28, said decoupling capacitor having a capacitance of approximately 50 nf/cm^2.

30. (Previously presented) The device according to claim 12, further comprising a plurality of decoupling capacitors mounted on said first surface.

31. (Previously presented) The device according to claim 12, further comprises at least one resistor mounted on said first surface.

32. (Currently presented) The device according to claim ~~12~~ 30, wherein each of said plurality of circuit devices is ~~are~~ in electrical communication with at least one of said decoupling capacitors.

33. (Cancelled)